

Millimetre-Wave Integrated Circuits for Radioastronomy and Telecommunications

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Abstract

CSIRO has contracted with TRW for two InP high electron mobility transistor (HEMT) wafer fabrication runs and one InP heterojunction bipolar transistor (HBT) wafer fabrication run.

The circuits on the HEMT wafers include:

- Wide-band, resistive HEMT mixers,
- Wide-band, low-noise MMIC amplifiers for radioastronomy and telecommunications,
- Wide-band bi-directional millimetre-wave amplifiers, and
- 100 GHz oscillators.

The circuits on the HBT wafers include:

- 40/20 GHz analogue frequency dividers,
- Wide-band, four quadrant, Gilbert cell analog multipliers,
- Vector modulators,
- Four-decade LOG-video amplifiers,
- Wide-band distributed amplifiers,
- High speed 3-level digitisers,
- Sigma-delta analog-to-digital converters,
- Wide-band, Schottky diode mixers,
- Direct-coupled DC – 30 GHz amplifiers,
- Transimpedance amplifiers with photo-diode input, and
- Phase/frequency detectors.

In this paper we will describe the design and performance of some of these circuits.

1.0 Introduction

Most millimetre-wave receivers currently used in radioastronomy are built using superconductor-insulator-superconductor (SIS) or Gallium Arsenide (GaAs) discrete components. Monolithic millimetre integrated circuits (MMICs) can replace all the discrete components of a receiver by a single chip which can be mass-produced, achieving cost savings and greater reproducibility and reliability. Arrays of receivers can be built using many such chips, allowing complex, multiple-beam receiving systems not otherwise possible. It is also feasible to cryogenically cool receiver arrays built using large numbers of MMIC chips because of their small size and lower thermal mass.

Indium phosphide (InP) technology has become the first choice for mm-wave devices and integrated photonic systems because of its lower noise, higher frequency response and superior cryogenic behaviour, and because of its intrinsic suitability for 1.5 micron photonic devices.

The wafers from the first HEMT fabrication run have been delivered and are undergoing on-wafer testing. The circuit designs for the HBT fabrication run have been delivered to the foundry for fabrication.

2.0 HEMT circuits

The MMIC HEMT circuits were designed for the advanced, 0.1 micron, InP HEMT process recently developed at TRW [1]. The circuits were realized using microstrip transmission lines, thin film capacitors (0.30 fF per square micron) and thin film resistors (100 ohms/square) on 75 mm diameter, 75 micron thick, indium phosphide substrates.

Commercial software, HP-EEsof Libra, was used for circuit simulations and for creating the chip layout automatically. The non-linear HEMT model was developed by CSIRO using bias-dependent on-wafer measurements of sample devices. Other process-dependent device models such as the via-hole, linear HEMT model and the HEMT diode were provided by TRW. A standard Schottky diode model was used to model the HEMT diode in the voltage-controlled oscillator circuit. This model was intended for mixer operation and the variable capacitance behaviour was not expected to be very accurate for varactor operation with large bias voltages. The micro-strip elements were modelled by standard Libra elements. Model libraries for auto-layout were developed by CSIRO using TRW design rules.

2.1 *Wide-band, resistive HEMT mixers*

A range of mixers was designed for the 30 – 50 GHz and 85 – 115 GHz frequency bands which are of interest to radioastronomy. The mixer designs include both double sideband mixers and image-reject mixers for each frequency band. Some of the image-reject mixers were designed for use with an off-chip IF hybrid and others were designed with an on-chip IF hybrid. The mixer designs also include second harmonic versions of some of the mixers for the 85 – 115 GHz frequency band.

Mixers for the 30 – 50 GHz frequency band were tested at fixed IF frequencies of 5 and 10 GHz. The conversion loss of the double sideband mixers was about 11 dB at both IF frequencies, with a local oscillator power of +2 dBm. The image reject mixers with an on-chip IF hybrid had a conversion loss of 11 dB at an RF frequency of 30 GHz, rising to 15 dB at 50 GHz, with a local oscillator power of +5 dBm. The image rejection was better than 15 dB for an IF frequency of 10 GHz.

Mixers for the 85 – 115 GHz frequency band were tested at a fixed local oscillator frequency of 100 GHz. The conversion loss of the double sideband mixers was 10 dB, with a local oscillator power of +2 dBm. The image reject mixers with an on-chip IF hybrid had a conversion loss of 12 dB and image rejection of better than 15 dB for IF frequencies in the range 7 – 15 GHz, with a local oscillator power of +5 dBm.

The measured conversion loss is typically 2 – 3 dB higher than that predicted by the simulation.

2.2 *Wide-band, low-noise MMIC amplifiers*

A number of low noise amplifiers were designed, including amplifiers for the 16 – 25 GHz, 30 – 50 GHz and 85 – 115 GHz frequency bands which are of interest to radioastronomy. As the lowest noise performance has been reported for cryogenically cooled amplifiers, we intend to cool these amplifiers, but the transistor models used for the design are only valid for

a range of temperatures around 25°C, and do not explicitly model device performance at cryogenic temperatures. Consequently, circuit performance was optimized using the (room temperature) models that were available.

The amplifiers for the 16 to 25 GHz and 30 to 50 GHz bands were designed for minimum noise across the band, with flat, 20 dB and 30 dB gain and input and output return losses better than -15 dB over the whole band, and better than 20 dB midband. The 16 to 25 GHz amplifiers were implemented as two- and three-stage designs to achieve 20 and 30 dB gain respectively. For the 30 to 50 GHz amplifier, a four-stage topology was utilised to achieve 30 dB gain. For these first-pass designs, good agreement was achieved between the predicted characteristics and the on-wafer measured amplifier performance, although in some circuits the noise figure is somewhat higher than in the simulation. The lowest noise figure measured in the two-stage 15 to 25 GHz band amplifier was 1.5 – 2.2 dB.

The primary goal for the 85 to 115 GHz amplifier was to achieve minimum noise in the band, with good input and output return losses and a nominal gain of 15 dB. Three variations of the amplifier circuit were designed. The best performance was achieved by a circuit with greater than 10 dB gain over the whole band. The performance of this amplifier will be described elsewhere. Typical performance of another circuit design is shown in Fig. 1(c). The noise figure of the amplifier, between 90 and 98 GHz, is shown in Fig. 1(d).

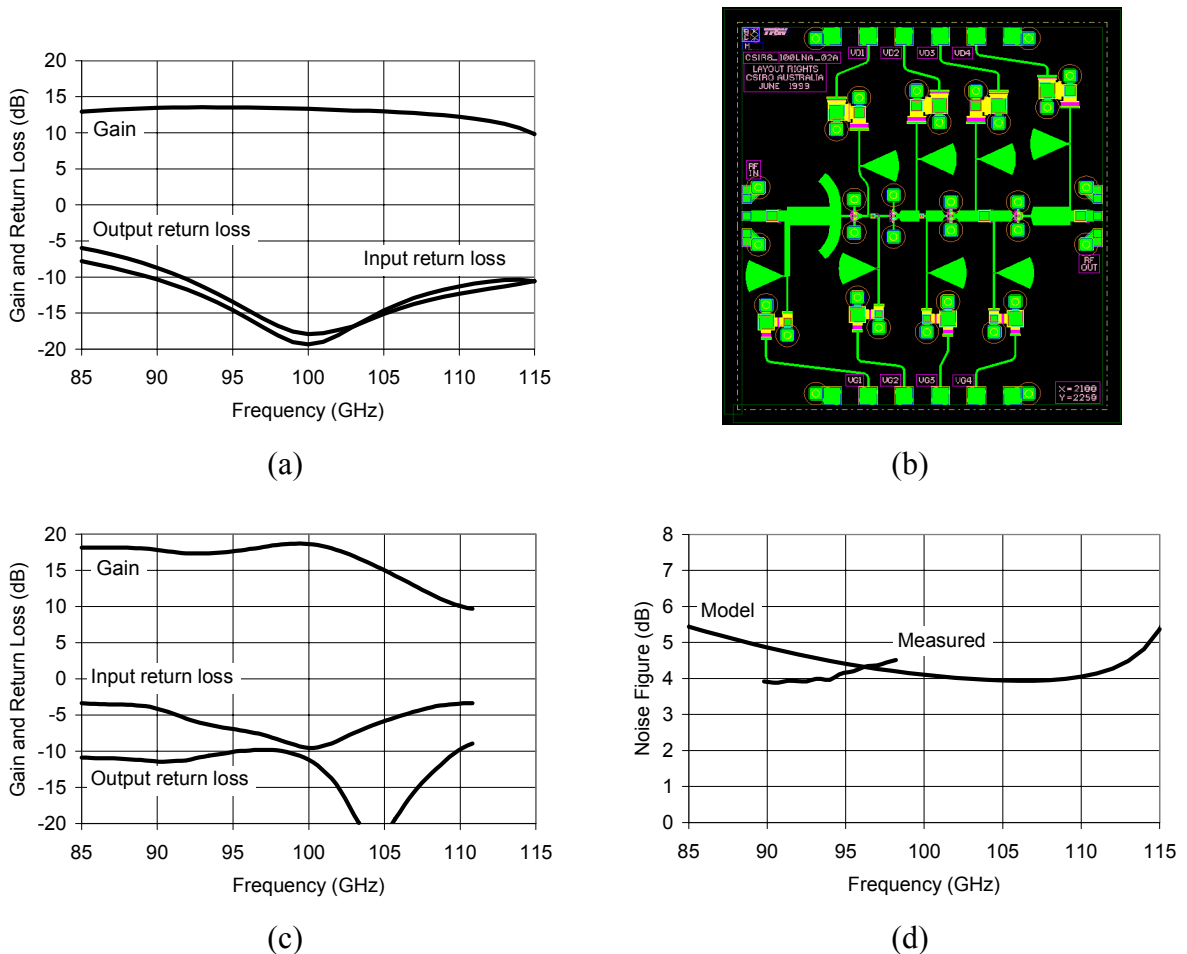


Fig. 1 85 - 110 GHz amplifier
 (a) simulated gain and match (b) amplifier layout
 (c) measured gain and match, (d) noise figure.

The estimated accuracy of the on-wafer noise figure measurement is ± 1 dB. The noise figure is similar to that predicted by the simulation.

2.3 Wide-band bi-directional millimetre-wave amplifiers

CSIRO has developed a patented¹ bi-directional amplifier (BDA) concept for monolithic microwave integrated circuit (MMIC) half-duplex transceivers [2], [3]. A BDA can substantially reduce the complexity of a transceiver system because it requires only a single signal path for both transmit and receive functions. The direction of operation of the BDA is easily reversed by changing the DC bias values. CSIRO's BDA circuit makes use of the drain-source symmetry inherent in common-gate-connected field-effect transistors. Input and output matching circuits are topological mirror images designed to achieve identical frequency response for forward and reverse operation. The earlier bi-directional amplifier designs [2] were potentially unstable due to common-gate-connected HEMT devices and had relatively narrow bandwidth.

A new wide-band bi-directional amplifier (BDA) circuit, with improved bandwidth, stability and input and output return losses, has been designed and measured. It was intended that the amplifier would cover the whole 40-60 GHz band. Between 40 and 56 GHz, greater than 8 dB gain and better than 18 dB input and output return loss have been achieved. It is expected that the BDA chips should function well at cryogenic temperatures.

2.4 100 GHz oscillators

Two InP HEMT oscillator circuits were designed and fabricated. Both designs are identical except for the frequency-setting elements. In the first design, an open-ended stub is used to create a fixed frequency oscillator. The second design includes a HEMT diode as a varactor, producing a voltage-controlled oscillator (VCO). The frequency of the oscillators was chosen to be 100 GHz for a radioastronomy application. It is expected that the oscillator chips should function well at cryogenic temperatures, possibly with better phase noise

Several examples of each circuit were measured on-wafer. The oscillator frequencies were between 99.5 and 102.1 GHz and the best output signal level was -6.3 dBm. The VCO circuits' tuning range varied, chip-to-chip, between 230 and 950 MHz. The average phase noise of the VCO and the fixed frequency oscillator circuits was -96.5 dBc/Hz and -98 dBc/Hz respectively at 10 MHz from the carrier. At room temperature, frequency of operation, output power and tuning range of the oscillators were found to show good agreement with simulated performance. This was a first pass design and the good performance means a second pass is unnecessary.

3.0 HBT circuits

The circuits described below were designed for the TRW 1 micron HBT process and are presently being fabricated.

3.1 40/20 GHz Analogue frequency divider

¹ Patented: Australia (678076), USA (5821813), and Taiwan (77067), Other Patents Pending

An analogue frequency divider, based on a 40 GHz HBT mixer with a 20 GHz bandpass feedback amplifier, has been designed. With a 40 GHz input signal, the output power at 20 GHz is expected to be +4 dBm. The predicted input return loss is better than -15 dB.

3.2 Wide-band, four quadrant, Gilbert cell analog multiplier

A Gilbert-cell, four quadrant multiplier, with a class-B power output buffer amplifier, has been designed. Over the DC - 35 GHz frequency range, the single ended inputs and outputs should have a return loss better than -10 dB, (relative to 50 ohms), and a maximum output power of +10 dBm. into 50 ohms. The predicted gain is 0 dB (from input (1) to output, with the alternate input (2) at +1 volt) with linearity better than 1% for a DC input voltage in the range ± 1 volt.

3.3 Vector modulator

A vector modulator, comprised of an inverting and non-inverting pair of Gilbert-cell four-quadrant multipliers with a differential-RF-inputs, has been designed. The multipliers are fed by a lumped element, 6-18 GHz quadrature network. The output is summed and amplified in a differential-input, class-B power buffer amplifier.

Over frequency range 6-18 GHz, the quadrature accuracy should be ± 1.5 dB, the amplitude flatness ± 1 dB and the conversion gain 0 dB. I and Q inputs are single ended, with a return loss better than -10 dB in the DC to 10 GHz operating band. The predicted amplitude variation for a 360 degree phase change is ± 1 dB.

3.4 Four-decade LOG-video amplifier

A four-stage, cascaded, true logarithmic video amplifier has been designed. The amplifier uses parallel-connected emitter-coupled pairs with a saturating gain characteristic. A class-B output buffer amplifier is used to provide a maximum output power + 10 dBm into 50 ohms. The amplifier will operate over a frequency range of DC to 15 GHz, with maximum and minimum gains per stage of 10 dB and 0 dB respectively. Over the operating frequency range, the input and output return losses are expected to be better than -10 dB, and the logging dynamic range greater than 40 dB.

3.5 Wide-band distributed amplifiers

Wide-band distributed amplifiers with at least 10 dB gain and better than -10dB input and output return loss were designed for the 4-28 GHz band.

3.6 High speed 3-level digitiser

A two-bit digitiser, with integrated demultiplexer, has been designed for operation up to 8 Giga-Samples/second. This circuit digitises the input signal at the full sample rate and then an on-chip 1-to-4 demultiplexer converts the output stream into 4 parallel outputs. Each output, at one quarter of the sampling rate, is designed to drive 50 ohm terminated lines at ECL levels, which can then be processed with slower speed commercial electronics. The circuit is designed to accept an input signal level of -6 dBm, and has a common mode range 0 to -1.3V. The clock and RF input signal lines are terminated on-chip with matched loads. A

variation of the high speed, 3-level, digitiser circuit, is designed to have the clock delivered by optical fibre and the outputs are designed to directly drive off-chip laser diodes.

3.7 *Sigma-delta analog-to-digital converter*

Sigma-delta ($\Delta\Sigma$) modulation is a technique which combines oversampling and filtering to perform analog-to-digital conversion. The noise from a low resolution quantizer is shaped away from the signal band, and is then removed, by filtering, in a following stage.

A high-speed sigma-delta ($\Delta\Sigma$) analog-to-digital converter has been designed. The circuit is a continuous-time first-order lowpass $\Delta\Sigma$ modulator which contains, in order, a transconductance cell, an integrator, a comparator with its clock, and a digital-to-analog converter. The digital-to-analog converter output is fed back to the integrator input. The simulation results are promising: we can sample a signal bandwidth of 50 MHz at a clock rate of 4 GHz with good results. Three sub-circuits will be fabricated: a clock, a clocked comparator and the first-order lowpass $\Delta\Sigma$ modulator.

3.8 *Wide-band, Schottky diode mixers*

Schottky diode mixers were designed for the 30 – 50 GHz and 85 – 115 GHz frequency bands. The mixer designs include both double sideband mixers and image-reject mixers for each frequency band. The image-reject mixers were designed with an on-chip IF hybrid.

3.9 *Direct-coupled DC – 30 GHz amplifier*

A true direct-coupled DC – 30 GHz amplifier has been designed with a differential-pair input stage and Darlington structure output stage. Multiple feedbacks were used to achieve simulated input and output return losses of better than –10 dB, and better than 10 dB flat gain.

3.10 *Transimpedance amplifier with photo-diode input*

A transimpedance amplifier, with photo-diode input, has been designed based on the direct-coupled DC – 30 GHz amplifier described above. The simulated gain of this circuit is better than 40 dB.

3.11 *Phase/frequency detector*

A differential input, phase/frequency detector has been designed with multiple AND gates, invertors and R-S flip-flops. It is expected that the circuit will operate at 2.5 GHz, with a linear detecting range of $\pm 270^\circ$ phase difference between the input and reference signals.

References

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- [3] John W Archer, Robert A. Batchelor and Oya Sevimli, “Millimetre-Wave Bi-directional Amplifiers”, *1997 Topical Symposium on Millimeter Waves*, pp. 19-22, Kanagawa, Japan, 7-8 July, 1997.