

Trap Related Current Lag Phenomena in Heterojunction Devices.

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Abstract

Current lag is a detrimental parasitic effect, which can seriously limit the performance of GaAs based device and integrated circuits. Gate lag affects digital circuits such as inverted chain, digital radio systems, the distortion characteristics of FET etc. Both gate lag and drain lag has been observed in Hetero Junction (HJ FET) devices. This lag is usually attributed to trap. We have carried out pulsed measurements to observe this current lag in HJFET devices. Gate lag is observed having more than one time constant. Although the cause of this current lag is thought to be due to surface state trap, further experiments are being carried out to verify this. The goal of this research is to develop an empirical model of surface state trapping in FET devices and hence to be able to predict the current lag.