Modelling electron trapping effects on gate lag in Field Effect Devices

Saif Uz Zaman and Anthony Edward Parker
Department of Electronics, Macquarie University, Sydney, NSW 2109, AUSTRALIA.
mailto: saif@ics.mq.edu.au

ABSTRACT

Traps at the surface of devices cause delayed response of drain current to a step change of gate voltage. This is known as gate lag. Gate lag is usually caused by surface hole trapping. Traps at the surface are charged negatively during turn-off of the device. The negative charge turns the device further off. After turn-on, these negative charges decay by means of capturing holes, which turns the device further on. However, measurements have shown that electron trapping also occurs during gate pulsing which causes drain current to decrease after turn-on pulse. This paper aims to model this electron trapping effect and combine it with a previously developed hole trapping model.