

CHARACTERISING MICROWAVE TRANSISTOR DYNAMICS WITH SMALL-SIGNAL MEASUREMENTS

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ABSTRACT

Small-signal microwave transistor characteristics are used to construct and fit a comprehensive model of their dynamic behaviour. The model includes thermal effects and trap-related effects, which influences such a large range of frequencies that they are not well characterized by large-signal or pulse measurements alone. Correlation of the model with small-signal characteristics demonstrates the region of influence of specific dynamic effects. The model extrapolates beyond the measurement space to quantify the very significant impact that transistor dispersion has on microwave circuit performance. The results question the adequacy of conventional transistor characterization techniques for accurate circuit design.

INTRODUCTION

Dynamic behaviour of transistors is the variation of the current-voltage characteristic with frequency and bias. This behaviour affects gain, intermodulation, and power efficiency of microwave circuits. When accounting for the dynamics in the design of circuits at microwave and millimetre-wave frequencies, transistor modeling is fundamentally problematic. This is because the behaviour of a transistor in a circuit can be very different to that for which its model was developed. For example, the dc characteristic, so commonly used to fit models, is markedly different to the 100ns pulse characteristics, which may be a better indication of a transistor's behaviour at high frequencies.

Out-of-band phenomena influences circuit performance significantly. The impedance of terminations, loads and bias networks, at base-band frequencies is one source of intermodulation asymmetry at microwave frequencies [1] [2]. The intrinsic terminal impedances of transistors at base-band frequencies is another [3]. Because temperature responds to changes in power at beat frequencies, it can influence in-band intermodulation [4]. Any model of a transistor, therefore, needs to describe dynamic behaviour over all frequencies rather than just the band of application.

Various measurement techniques have been employed to determine the details of the dynamic behaviour. Measured output conductance shows a reduction as frequency increases, which crudely can be modeled by single-time-constant networks. A change in apparent dc characteristics with measurement speed has led to the development of pulsed and step-transient measurements, which reveal the change in drain current over time as a transistor is switched from one bias to another [5]. These show clearly the effects of impact ionization, which causes gate-lag — a delayed increase in drain current as the transistor is turned on [6]. They also show drain-overshoot — an initial high current that settles over time — that has been attributed to electron trapping and self-heating. Measurement of small-signal characteristics shows effects that can be correlated with pulse characteristics but extend to frequencies far beyond the speed of pulse systems [7]. These measurements, of intrinsic gain and intermodulation, show that dispersion has an effect over the whole spectrum from dc to $\gg 10$ GHz.

The variation of a transistor's intrinsic gain and intermodulation with bias exhibits a structure that is clearly a function of several dispersion effects. An initial attempt, which used extremely crude models, demonstrated the possible links between transistor dynamic behaviour and the mechanisms of self-heating, impact ionization, and electron trapping [8]. However, the exact separation of these phenomena was flagged for further investigation.

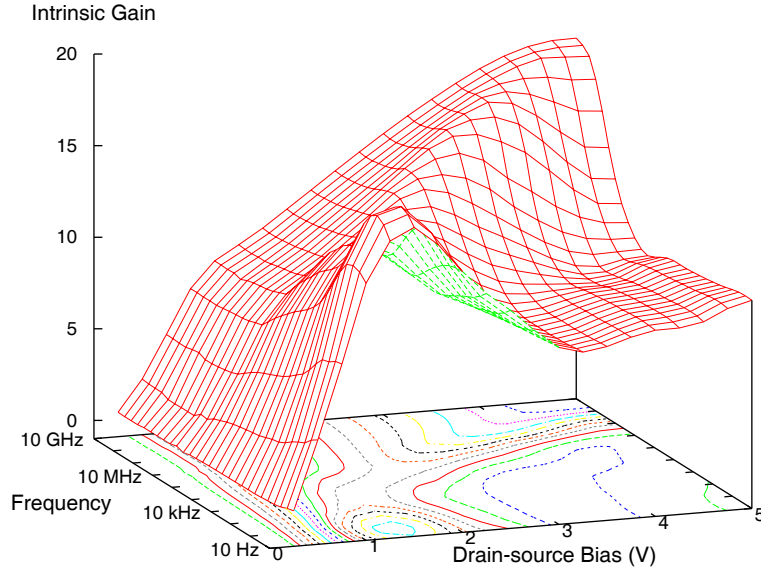


Fig. 1. Magnitude of intrinsic gain of a pHEMT biased at a gate-source potential of -0.8 V (about 50% I_{DSS}). This device is $160\ \mu\text{m}$ wide and has a breakdown at $V_{GD} < -10$ V. This surface exhibits the salient features of shape and magnitude that those at other gate-source biases exhibit, included those near pinch-off.

This paper details the process of building a dynamic model of a HEMT based on a better understanding of the dispersion effects. The next section defines intrinsic gain and its measurement over the whole spectrum. The following section then describes the dynamics of intrinsic gain in terms of better models of heating, impact ionization and electron trapping. This includes a description of the time constants of each and their bias dependence. The penultimate section uses the model to quantify the impact of dispersion on the nonlinear properties of the transistor. The conclusion is not just that these effects are significant but that they are also critically bias- and frequency-dependent, so a comprehensive characterization is essential.

INTRINSIC GAIN

Intrinsic gain is a figure-of-merit that identifies the potential performance of a transistor technology. It is useful because it is independent of scaling with respect to gate width and is relatively easy to measure.

In the context of this work, the intrinsic gain of a transistor A_i at frequency ω can be defined in terms of real parts of its y -parameters as:

$$A_i(\omega) = \frac{\Re(Y_{21}(\omega))}{\Re(Y_{22}(\omega))}. \quad (1)$$

This is the ratio of transconductance g_m to drain-source conductance G_{ds} and is the voltage gain that the transistor can deliver in common-source configuration into an open-circuit load.

Vector network analyser measurements over a range of bias and frequencies can be routinely obtained and provide the y -parameters. For modeling purposes, it is necessary to transfer the measurements to the internal nonlinearity of the device. There are well established methods for determining the access resistances, capacitances and inductances and remove them from the data [9] [10].

To reveal the full dynamic behaviour of the internal nonlinearity, it is necessary to investigate a full spectrum from a few cycles-per-second to beyond the f_t of the device. In some technologies, such as GaN, and early-stage technologies, the dynamics can occur at sub-one-hertz frequencies. However, the directional couplers in network analysers impose a lower limit ranging from 300 kHz to 50 MHz typically. Thus it is necessary to measure gain at lower frequencies using other techniques. Transconductance and gain can be extracted from several step responses to the neighbourhood

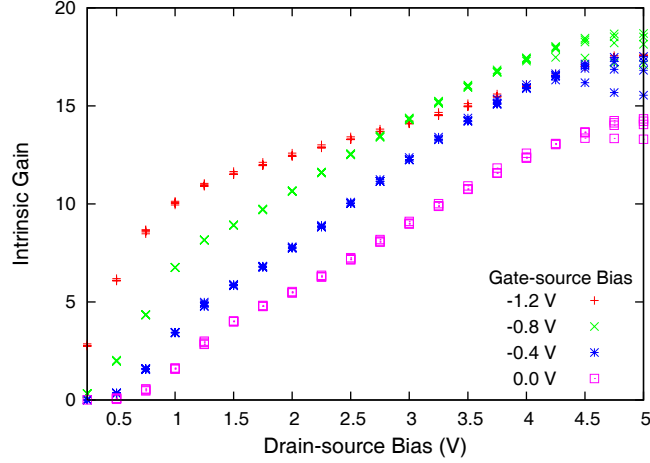


Fig. 2. Magnitude of *isodynamic* intrinsic gain of the same pHEMT in Fig. 1. This is the data at 1, 3, 5 and 10 GHz for four gate-source potentials (one of which is that of Fig. 1). These are considered *isodynamic* because they are constant with respect to increasing frequency.

of a bias point [8]. A network analyser that uses a resistive bridge can cover very low frequencies, down to dc [11].

The data from an RF network analyser and low frequency gain measurement can be stitched together to give a complete picture of frequency dependence, as shown in Fig. 1.

Isodynamic Intrinsic Gain

It is apparent in Fig. 1, which shows the measured intrinsic gain of a microwave pHEMT, that there is a significant variation in gain with bias and frequency. The variation is exhibited over all frequencies up to many GHz at high drain bias. However, for any drain bias there exists a frequency above which there is little variation in intrinsic gain. It is reasonable to expect that the gain – a ratio of real components of y -parameters — remains constant to beyond 100 GHz since it is only one more decade beyond the nine decades shown in Fig. 1. Measurements to 30 GHz have confirmed this, albeit with increasing dominance from the imaginary components.

The constancy of intrinsic gain with increasing frequency is well demonstrated in Fig. 2, which shows this at frequencies above 1 GHz for several gate-biases. Near the 5V drain-source bias the gain is constant above 5 GHz. Because these high-frequency measurements are frequency independent, it can be assumed that trapping and heating phenomena remain static during the measurement. The gain in this region is termed *isodynamic* because it not affected by ‘low-frequency’ effects.

A model of transistor dynamics can be constructed with a core description of the isodynamic characteristics that is controlled by additional descriptions of trapping and heating. The latter can be assumed to be constant bias offsets or scaling when considering the isodynamic core description.

Although there are many types of MESFET and HEMT models, they share a common structure for their drain-current description in the saturated region, which is

$$i_D = f(v_{GS} + g(v_{DS})), \quad (2)$$

where f and g are functions with various forms, depending on the model.

The intrinsic gain predicted by this model is

$$A_i = -\frac{g_m}{G_{ds}} = -\frac{\frac{d}{dv_{GS}} i_D}{\frac{d}{dv_{DS}} i_D} = -\frac{\frac{df(x)}{dx}}{\frac{df(x)}{dx} \frac{dg}{dv_{DS}}} = \frac{-1}{\frac{d}{dv_{DS}} g(v_{DS})}. \quad (3)$$

For most models $g(v_{DS}) = \gamma v_{DS}$, which gives a constant intrinsic gain of $A_i = -1/\gamma$. However, in the saturated region ($v_{DS} > 1$ V), the measured isodynamic gain is observed to be a linear function of drain bias. This is also true

for MESFETs. Thus, a suitable expression for the modulation function is:

$$g(v_{DS}) = \frac{1}{m} \ln \left(\frac{m}{A_o} v_{DS} + 1 \right), \quad (4)$$

which gives

$$A_i = \frac{-1}{\frac{d}{dv_{DS}} g(v_{DS})} = -(m v_{DS} + A_o), \quad (5)$$

where m and A_o are the slope and intercept of the isodyanmic gain that can be estimated from Fig. 2. (Note that Fig. 2 shows $-A_i$ since a common-source amplifier has an inverted output.) The predicted intrinsic gain depends on the structure of the function $f()$ in (2) and bias offsets applied by trapping and thermal descriptions, so there will be a need to optimize m and A_o . Also, near $v_{DS} = 0$ the gain reduces as the transistor enters its linear region of operation. This is dictated by the structure of $f()$ with little impact from $g()$.

DYNAMICS OF INTRINSIC GAIN

As frequency decreases, the intrinsic gain varies considerably through the actions of three dominant processes. These processes are self-heating, trapping of negative charge, and trapping of holes generated by impact ionization. The dominance of these has been previously demonstrated with crude descriptions [8]. However, the correct regions of bias and frequency and their true impact remained a subject of further investigation. In particular, it was difficult to separate heating and trapping because they both produce a reduction in drain current.

The following takes each effect in turn and examines their influence on intrinsic gain.

Self Heating

A transistor dissipating power undergoes heating and there is a reduction in its drain current as temperature rises, because of the temperature dependence of saturated velocity. Static self-heating can be implemented as

$$I_{DS} = \frac{i_D}{1 + \delta v_{DS} i_D}, \quad (6)$$

where δ is the heat capacity-thermal coefficient product for the process, and i_D is given by (2).

This gives a static (that is $\omega = 0$) intrinsic gain of

$$A_i = -\frac{g_m}{G_{ds} - \delta i_D^2}, \quad (7)$$

where g_m and G_{ds} are the transconductance and output conductance of i_D . As power dissipation increases the intrinsic gain is also increased because the total output conductance is reduced.

A frequency-dependent model of the heating process can be implemented by convolving the instantaneous power dissipation with the thermal impulse response of the device. In the frequency domain this response is

$$H(\omega) = \frac{1}{(1 + j\omega/\omega_o)^n}, \quad (8)$$

where ω_c is the characteristic frequency of heating and n is the order of the process. For zero frequency, the convolved power dissipation and the instantaneous power are the same. For frequencies well above ω_o the convolved power becomes the average power at the bias point. The latter is constant and does not influence the intrinsic gain.

Modeling self heating and extracting its parameters from intermodulation measurement has been well documented [4]. Thus it is possible to confidently identify the region of influence on intrinsic gain that self-heating has. The values of ω_c and n are 50,000 rad/s and 0.35 respectively for the device in Fig. 1. Thus any observed increase in gain can only be attributed to self heating if it occurs at frequencies below 10 kHz, which is the region indicated on the contour plot of Fig. 3.

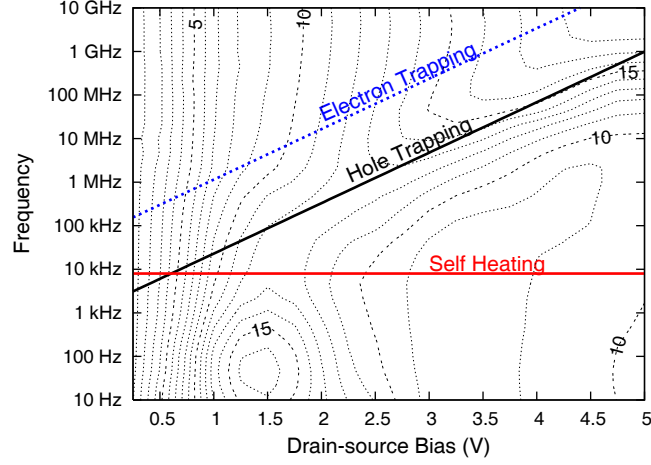


Fig. 3. Frequencies of influence for trapping and heating mechanisms superimposed on a contour plot of the intrinsic gain in Fig. 1. Any significant departure from isodynamic gain can be attributed to each effect only at frequencies near of below the corresponding line.

Trapping of Negative Charge

Negative charge trapped at the surface or within a transistor will contribute to a depletion of current carriers that reduces drain current. The effect of increased negative charge can be modelled by subtracting a *trap potential* from the gate terminal potential as follows:

$$i_D = f(v_{GS} - v_e(v_{GS}, v_{DS})) + g(v_{DS}), \quad (9)$$

where v_e is a bias- and frequency-dependent potential of trapped negative charge. This potential could result from either trapping of electrons or a reduction in trapped holes. The magnitude of either of these is increased by a more-negative gate terminal potential.

A candidate function for v_e is

$$v_e = V_{EO}s \ln \left(\exp \left(\frac{\phi - v_{GS} + \phi - v_{GD}}{s} \right) + 1 \right), \quad (10)$$

where V_{EO} is a trapping potential constant, s is a smoothing parameter, and ϕ is a positive potential related to the maximum gate-junction forward bias. Suitable values that fit the data of Fig. 1 for these parameters are 50 mV, 200 mV, and 900 mV respectively.

This function for v_e is zero when the gate is forward biased with respect to both the source and drain, which is akin to having an ungated channel. It is only when the gate is negative with respect to the channel that a trap potential proportional to V_{EO} is produced. The log/exp nesting limits the potential to zero if a high forward bias is applied, which can occur during intermediate iterations in a simulation.

The static intrinsic gain (at $\omega = 0$) is given by

$$A_i = - \frac{1 - \frac{d}{dv_{GS}} v_e}{\frac{d}{dv_{DS}} g(v_{DS}) - \frac{d}{dv_{DS}} v_e}, \quad (11)$$

which is greater in magnitude than the isodynamic gain. Moreover, this increase in gain is substantial at low drain biases where the isodynamic gain is less significant (that is, where $\frac{dg}{dv_{DS}}$ nears $\frac{dv_e}{dv_{DS}}$).

The boost in intrinsic gain at extremely low frequencies is clearly evident near $v_{DS} = 1.5$ V in Fig. 4. Although this at a frequency that is affected by self-heating, the increase in gain due to self-heating is less at low drain biases because power levels are low. Note that the large reduction in gain at higher biases is due to the dominance of positive charge trapping, discussed below.

There is an increase in intrinsic gain along the line labelled ‘electron trapping’ in Fig. 3. This is attributed to negative charge trapping because it has been established by independent means that heating is much slower. The characteristic

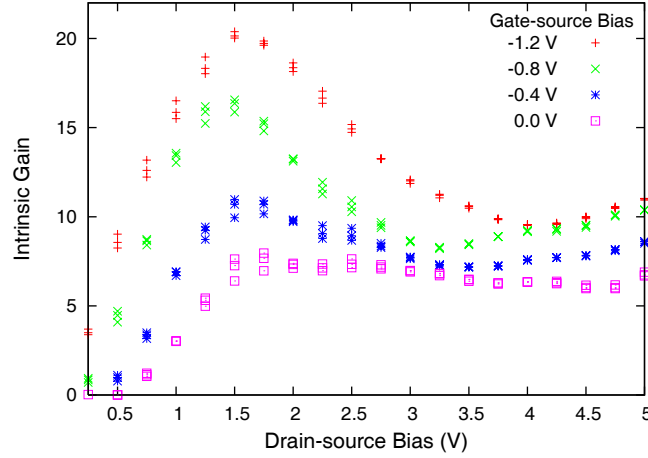


Fig. 4. Magnitude of *static* intrinsic gain of the same pHEMT in Fig. 1. This is the data at 10, 20 and 50 Hz for four gate-source potentials (one of which is that of Fig. 1). These are considered approximately *static* because the test frequencies are so low.

frequency of the electron trapping mechanism is

$$\omega_e = \omega_E \exp\left(\frac{v_{DS}}{V_E}\right), \quad (12)$$

where ω_E and V_E are fitting parameters, which for Fig. 3 are 500 krad/s and 375 mV respectively.

Trapping of Positive Charge

A dominant source of positive charge trapping has been identified as impact ionization [6]. The mechanism starts with an increase in drain current due to carriers ionizing electrons by impact and thus creating extra carriers. The rate of ionization is given by

$$r_i = A \exp\left(-\left(\frac{2B}{v_{DS} + \sqrt{v_{DS}^2 + Z^2}}\right)^M\right), \quad (13)$$

where A , B and M are fitting parameters and Z sets the rate at which the argument of the exponential is prevented from overflowing.

The resulting drain current, including the effect of self heating, becomes

$$i_{DS} = \frac{i_D}{1 + \delta P}(1 + r_i), \quad (14)$$

where P is the instantaneous power convolved with the thermal step response. This gives a slight increase in drain current at a critical drain potential.

However, the observed increase in drain current is substantially more because for each ionized electron, there is a hole traveling in the reverse direction. The holes can be captured (or recombined with a captured electron) to build up a net positive charge that assists the turn on of the channel. The effect of increased positive charge can be modelled by adding a *trap potential* to the gate terminal potential as follows:

$$i_D = f(v_{GS} + v_h(v_{GS}, v_{DS}) - v_e(v_{GS}, v_{DS}) + g(v_{DS})), \quad (15)$$

where v_h is a bias- and frequency-dependent potential of trapped positive charge.

A candidate function for v_h is

$$v_h = V_{HO} \ln\left(1 + \frac{r_i i_{DS}}{I_{HO}}\right), \quad (16)$$

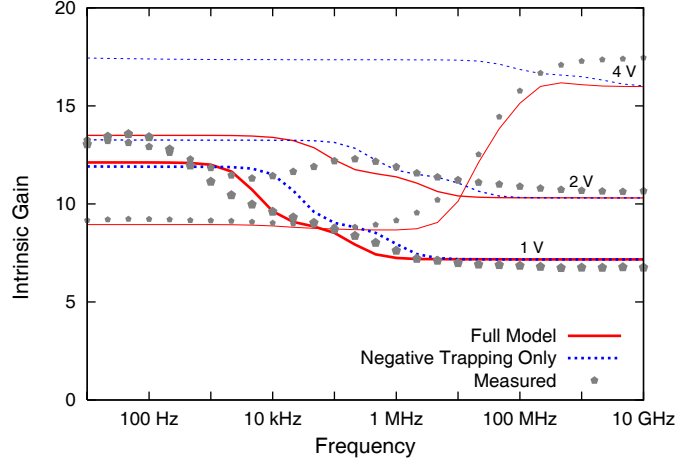


Fig. 5. Measured and modelled intrinsic gain for selected drain-source biases (as indicated) at a gate-source bias of -0.8 V. The smaller points and thinner lines are for higher drain bias. Note that heating is not a significant effect for this device at these biases.

where V_{HO} is a trapping potential constant and I_{HO} is current normalization constant. Suitable values that fit the data of Fig. 1 for these parameters are 30 mV and 200 nA respectively. (The values of A , B , M , and Z were set to 0.015, 7 V, 2, and 0.25 V respectively.)

The static intrinsic gain is significantly reduced by the positive-charge trapping mechanism. This is opposite to negative charge trapping because the charge has an opposite potential. Thus any reduction in intrinsic gain at low frequencies can be attributed to positive charge trapping. The effect is greatly reduced in bias regions or devices that do not exhibit the impact ionization *kink*.

The characteristic frequency of the positive-charge trapping mechanism is easily identified as the frequency below which there is a reduction in intrinsic gain. This is found to be

$$\omega_h = \omega_H \exp\left(\frac{v_{DS}}{V_H}\right), \quad (17)$$

where ω_H and V_H are fitting parameters, which for Fig. 3 are 10 krad/s and 375 mV respectively.

The difference between ω_E and ω_H is just the relative speed of the trapping processes.

FREQUENCY DOMAIN RESPONSE

The heating effect is a sub-first-order phenomena because the process involves a distributed network of heat capacity and thermal resistance throughout the volume of the transistor. It is easy to model the response in the frequency domain with (8), which can be entered directly into a frequency-domain simulator. In a time-domain simulator, it is necessary to construct a ladder network to model the distributed system [4].

Each trapping process can be modeled by a voltage source given by (10) (or (16)), charging a fixed capacitance through a variable resistance that gives the time constant appropriate for (12) (or (17)). The time constant is therefore set by the instantaneous drain-source potential, so that it is faster for a transient at a higher potential than a transient in the opposite direction. This is consistent with the transient dynamics observed with pulse measurements [5].

The frequency-domain view in Fig. 5 shows that the trapping processes are also sub-first-order in response. That is, the slope of gain versus frequency is less than 6 dB/octave. The figure shows a simulation with all three dynamic effects and another with negative charge trapping only. The latter has been implemented with a two-stage resistor/capacitor ladder (both resistances varying with bias) to stretch the response. A smoother and more-stretched response can be achieved with more stages [4].

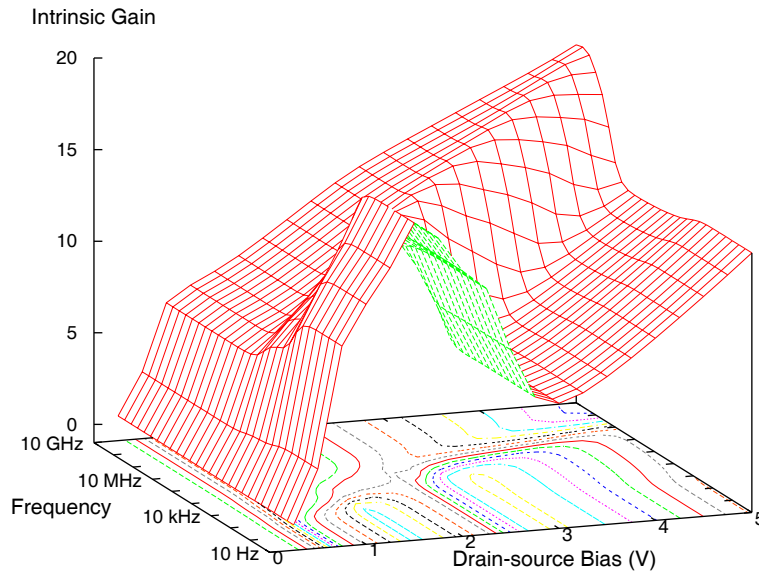


Fig. 6. A simulation of the intrinsic gain surface shown in Fig. 1. The simulation captures the salient features of the measurements but their frequency ranges are confined by the simple single-pole implementation used.

IMPACT OF DYNAMIC EFFECTS

A simulation of intrinsic gain using the descriptions given above is shown in Fig. 6. It exhibits the full structure of the measured data in Fig. 1 and matches the data quite well. A symmetric HEMT drain-current model was used as the core drain-current description ($f()$ in (2)), which is described in [12].

Note that the simulation is based on a relatively simple model that gives single-pole frequency-domain responses. This gives the simulated data a cleaner look than that of the measurements. However, it correctly predicts isodynamic gain, an increase in gain due to electron trapping and, at a lower frequency, the minor increase in gain due to heating, and the substantial drop in gain due to hole trapping, which corresponds to the occurrence of impact ionization.

Previous attempts at performing this simulation placed too much emphasis on heating [8]. The peaking in gain at low drain bias and low frequency was also unexplained, but now can be linked to the actions of negative charge trapping.

Intermodulation

The simulation can be used to assess the impact of the dynamic effects on intermodulation. Two significant contributors to third-order intermodulation are the third-order nonlinearity of the drain current and the second-order nonlinearity, which interacts with difference frequencies and causes intermodulation asymmetry [1] [2].

The relative level of the third-order nonlinearity is shown in Fig. 7. The surface of the third-order component in the isodynamic saturated operating region (1 to 10 GHz near the 3V drain-source bias) is fairly flat. Thus the value in that region has been used to normalize the data in the figure. The graph shows that there can be a ten-fold (20 dB) change in the third-order contribution near the characteristic frequencies of charge trapping and an even greater variation at low frequencies and low drain bias. The implications of this include the following:

- The characteristics of the transistor measured with dc or pulse data, which are restricted to less than 10 MHz, will not be an accurate predictor of intermodulation at 1 GHz or above.
- A distortion measurement at a particular frequency, say 1 GHz, cannot necessarily be used to predict intermodulation at higher frequencies unless the drain bias is low.
- Low-frequency operation at low bias is particularly sensitive to bias variations and exhibits several nulls and peaks, which are not present at GHz frequencies.

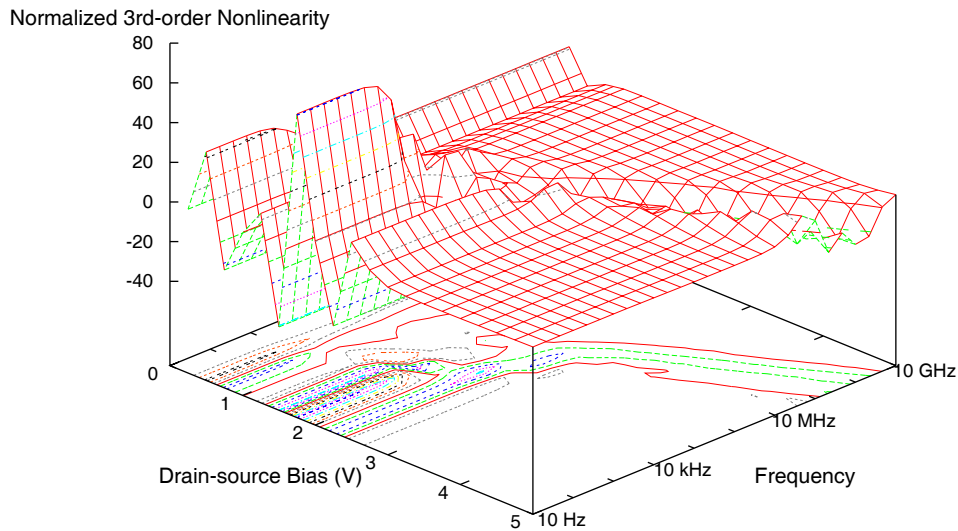


Fig. 7. A simulation at a -0.8V gate bias of the third-harmonic output for normalized to that at 10 GHz for a drain bias of 3 V. This shows the third-order nonlinearity relative to that of the isodynamic characteristic.

The relative level of the second-order nonlinearity is shown in Fig. 8. This is a simulation of the second-harmonic output normalized to that in the region of 1 to 10 GHz at the 3V drain-source bias. The graph shows that there can be a two-fold (6 dB) change with frequency.

The second-order nonlinearity contributes to the asymmetry between the upper and lower third-order intermodulation. A common scenario is a wide-band signal on a microwave carrier. The intermodulation levels are set by the third-order nonlinearity at the carrier frequency and the second-order nonlinearity at the base-band frequencies. Any variation in the second-order nonlinearity across the base-band will produce a corresponding variation in the intermodulation. The implications include the following:

- If the bandwidth of the base-band signal is less than 10 MHz, then the effect of the second-order nonlinearity will be invariant at higher drain potentials.
- Wider bandwidths will excite the second-order response at the characteristic frequencies of trapping and produce a variation in intermodulation. This can be detrimental to distortion-cancelling schemes that may be employed.
- A second-order distortion measurement at a particular frequency, say 1 GHz, cannot necessarily be used to predict intermodulation across any band of signal.

CONCLUSION

The nature of the dominant sources of the dynamic behaviour of HEMTs and MESFETs have been quantified. They are self-heating and positive and negative charge trapping. The two trapping mechanisms need to be considered separately because they have opposite effects and different characteristic frequencies. Heating, which has been considered significant, is shown to have only a minor effect on the small-signal parameters. It is important to consider the regions of influence of the dynamic effects when correlating characteristics measured in one regime with the performance of a circuit operating at another.

ACKNOWLEDGEMENTS

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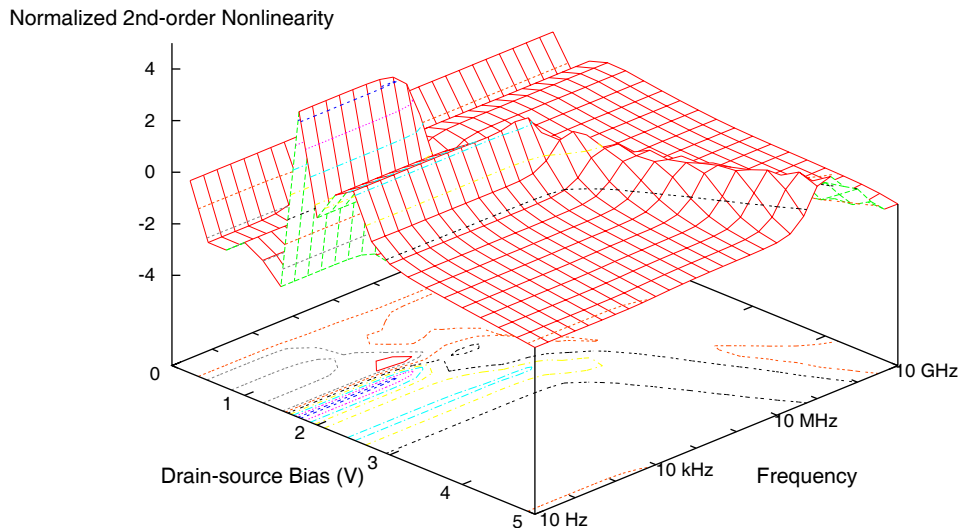


Fig. 8. A simulation at a -0.8V gate bias of the second-harmonic output normalized to that at 10 GHz for a drain bias of 3 V. This shows the second-order nonlinearity relative to that of the isodynamic characteristic.

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