

# Modelling electron trapping effects on gate lag in Field Effect Devices

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## ABSTRACT

Traps at the surface of devices cause delayed response of drain current to a step change of gate voltage. This is known as gate lag. Gate lag is usually caused by surface hole trapping. Traps at the surface are charged negatively during turn-off of the device. The negative charge turns the device further off. After turn-on, these negative charges decay by means of capturing holes, which turns the device further on. However, measurements have shown that electron trapping also occurs during gate pulsing which causes drain current to decrease after turn-on pulse. This paper aims to model this electron trapping effect and combine it with a previously developed hole trapping model.

## INTRODUCTION

Dynamic behaviour of Field effect device is affected by trapping. In the time domain, trapping effects are manifested as current lag [1], [2], [3], [4]. In frequency domain the equivalent effect is transconductance and drain conductance dispersion [5], [6]. Gate lag has an adverse effect in both analog and digital application [7]. Though surface state hole traps are the major cause of gate lag, simulations have shown that the influence of electron traps cannot be ignored [4]. Electron traps cause a small decrease of drain current immediately after a turn-on transient of the device.

This paper reports the modelling of this electron trapping effect in the gate lag of devices. This model is added to a previously reported hole trap caused gate lag model [8] to completely predict turn-on drain current transient. In the next section, drain current transient measurements are shown to identify the effects of hole trapping and electron trapping in gate lag. Then, the previously reported hole trapping related gate lag model is discussed briefly. The development of the electron trapping model for gate lag is discussed in the following section. Then, test simulation results of the combined hole and electron trap model are demonstrated.

## GATE LAG MEASUREMENTS

An NEC HEMT NE3210S01 was tested with an arbitrary pulsed semiconductor parameter analyzer (APSPA) [9]. To observe the turn-on gate lag, the device was turned on from off condition at various drain voltages. Figure. 1 shows the drain current transient for a gate turn-off voltage  $V_{G\text{OFF}} = -1.2$  V and various drain voltages.

It is seen that drain current is lower than its dc value immediately after the application of gate turn-on pulse and attains its dc value after some delay. This delay decrease with increasing drain voltage. The variation of delays is from 10ms to 1us for drain voltage from 1 V to 2.4 V. However, it is also seen that there is a slight decrease of drain current immediately after the application of turn-on pulse.

## HOLE TRAPPING MODEL AND SIMULATION RESULTS

When the gate is turned off, by an applied negative gate voltage, all the traps at the surface acquire negative charge [10]. After the gate is turned on, the negative charge decays slowly as the traps capture holes from the channel. Because of the presence of negative charge, the drain current cannot attain its dc value instantly. As the negative charge decays by capturing holes, the time constant is related to the number of available holes in the channel. The trapped negative charge gives rise to an additional negative voltage at the gate of the device. This is referred to as hole trap voltage in this paper.

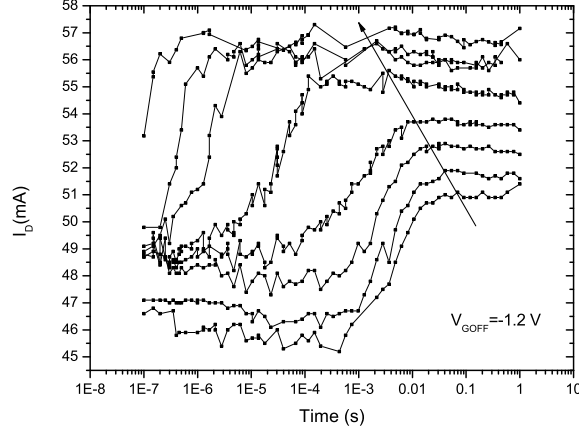


Fig. 1. Measured drain current transient, gate turned on from  $V_{GOFF} = -1.2$  V. Drain bias increasing in the direction of arrow from 1 V to 2.4 V in steps of 0.2 V.

The hole trap voltage is the reason behind for the delay in drain current with respect to pulsed gate voltage. Availability of holes in the channel depends on drain voltage, so time constant associated with hole trapping, hence the delay depends on drain voltage. Gate lag measurement for gate turned on from  $V_{GOFF} = -1.2$  V is seen in Fig. 1. Considering this physical mechanism, hole trap related gate lag model has been developed as described in [8]. For convenience of understanding the model is briefly discussed here. The trapping subcircuit consists of a nonlinear voltage dependent voltage source and a nonlinear RC filter. The voltage dependent voltage source is given by,

$$F(v_{GS}, v_{DS}) = K_1 + K_2 \frac{v_{GS}}{1 + e^{\frac{v_{DS} - P}{Q}}} \quad (1)$$

Where  $v_{GS}$  and  $v_{DS}$  are gate and drain voltage respectively. While  $K_1$ ,  $K_2$ ,  $P$ ,  $Q$  are fitting constants. Trapping time constant is given by a nonlinear drain voltage dependent resistance and a capacitor. The nonlinear resistance  $R_d$  is given by,

$$R_d = a v_{DS}'^{(b + c v_{DS}')} \quad (2)$$

$a$ ,  $b$  and  $c$  are arbitrary constants.  $v_{DS}'$  is to limit  $v_{DS}$  to a minimum value  $v_{DO}$  at a rate set by  $\sigma$ , and is given by,

$$v_{DS}' = \sigma \ln \left[ 1 + e^{\left( \frac{v_{DS} - v_{DO}}{\sigma} \right)} \right] + v_{DO} \quad (3)$$

## ELECTRON TRAPPING MODEL

In Fig. 1, it is seen that the drain current transient shows a slight initial fall specially at low drain voltages ( $V_{DS} < 1.6$  V). This is because of the small number of electron traps that capture the channel electrons after gate turn-on pulse [11]. So there is another trap voltage associated with electron trapping that is in opposition to the hole trapping voltage. For lower drain voltages as the hole trapping time constant is long, this current decrease is observable, but for higher drain voltages hole trapping time constant decrease and it obscures the electron trap related current fall. However, for significantly high drain voltage ( $V_{DS} > 2.1$  V) hole trapping time constant is so short that hole trapping precedes electron trapping, so drain current shows a slight fall after the hole trap related current rise finishes. Figure. 2 clearly shows these effects for three drain voltages. For  $V_{DS} = 1$  V, hole trapping time constant ( $\tau_h$ ) is greater than electron trapping time constant ( $\tau_e$ ). So hole trap related current rise starts after electron trap related current fall finishes. For  $V_{DS} = 2$  V,  $\tau_h$  is equal to  $\tau_e$ , so the current fall is obscured by the current rise. For  $V_{DS} = 2.4$  V,  $\tau_h$  is smaller than  $\tau_e$  so the electron trap related current fall begins after the end of hole trap related current rise. Variation of  $\tau_h$  and  $\tau_e$  with drain voltage for a gate turn-off voltage is seen in Fig. 3.

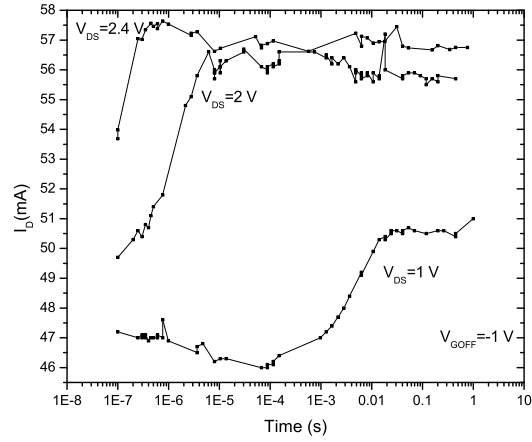


Fig. 2. Drain current transient for three different  $V_{DS}$  and  $V_{GOFF} = -1$  V.

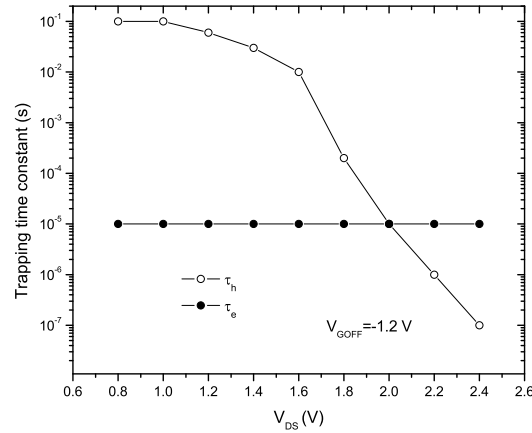


Fig. 3. Variation of electron and hole trapping time constant with  $V_{DS}$  for  $V_{GOFF} = -1.2$  V.

The time constant related to electron trapping has been found to be independent of drain voltage, which is consistent with previous investigation [12]. The electron trapping voltage is modelled as,

$$F'(v_{GS}) = \alpha v_{GS} \quad (4)$$

The combined model is seen in Fig. 4. As electron trapping time constant is found to be constant a fixed  $R = 10\Omega$  and  $C = 1\mu F$  is used in the simulation. It is seen in Fig. 4 that hole trap voltage and electron trap voltage are of opposite polarity as hole capture gives rise to current increase while electron trap results in current decrease during the turn-on transient. The variation of the function  $F'(v_{GS})$  for electron trap model and  $F'(v_{DS}, v_{GS})$  with drain voltage for several  $V_{GOFF}$  is seen in Fig. 5.

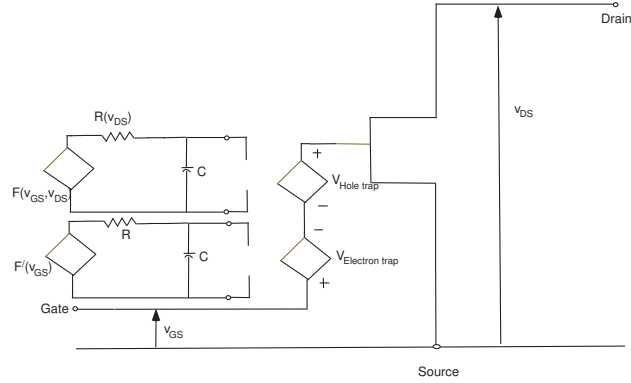


Fig. 4. Combined electron and hole trap model

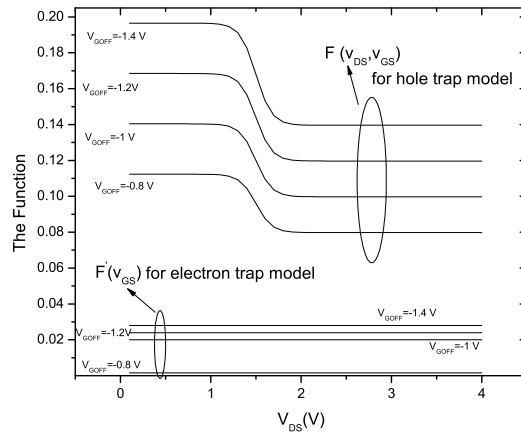


Fig. 5. Variation of  $F$  (hole trap model) and  $F'$  (electron trap model) with  $V_{DS}$ .  $V_{GOFF}$  is a parameter.

## SIMULATION RESULTS

To simulate drain current transient the combined hole and electron trap model has been used. Model parameters were extracted from Fig. 1 and the simulation result is seen in Fig. 6. Test simulation of the combined model has been done for gate turned on from several turn-off voltages  $V_{GOFF}$  as seen in Fig. 7–9. Measured data are shown as symbols while simulated data are shown as solid lines. The figures show that the combined model can predict the gate lag effect including the initial current decrease fall for all the gate turn-off voltages. Parameter values for the simulation are given in Table: I.

## CONCLUSION

Gate lag is primarily caused by surface hole traps, but electron traps also contribute to the behaviour of turn-on drain current transient. Electron traps cause slight decrease of drain current during the turn-on transient. The time constant associated with this trapping has been found to be constant for at least normal operation mode of the device. This electron trapping effect has been modelled and added with a previously developed hole trap model. It has been found that the combined model can predict the behaviour of drain current transient caused by trapping. At present the model's behaviour in frequency domain is being examined. Trapping is known to affect third order intermodulation component [13], [14].

TABLE I  
THE VALUES OF PARAMETERS USED IN SIMULATION.

Parameter	Value
$K_1$ (hole trap)	0.099717
$K_2$ (hole trap)	0.040674
P (hole trap)	1.49926
Q (hole trap)	0.08792
a (hole trap)	28530
b (hole trap)	7.448
c (hole trap)	-9.667
$v_{DO}$ (hole trap)	1
$\sigma$ (hole trap)	0.08
$\alpha$ (electron trap)	0.02

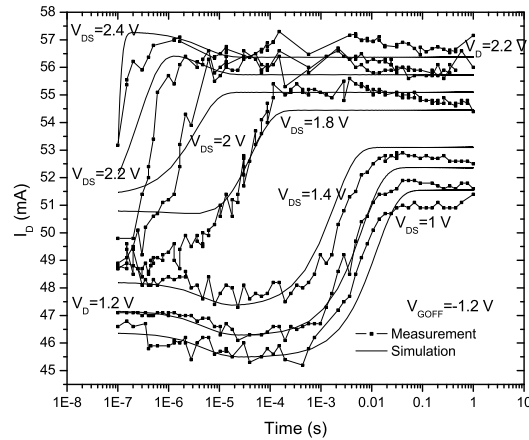


Fig. 6. Comparison of simulated and measured drain current transient for  $V_{GOFF} = -1.2$  V.

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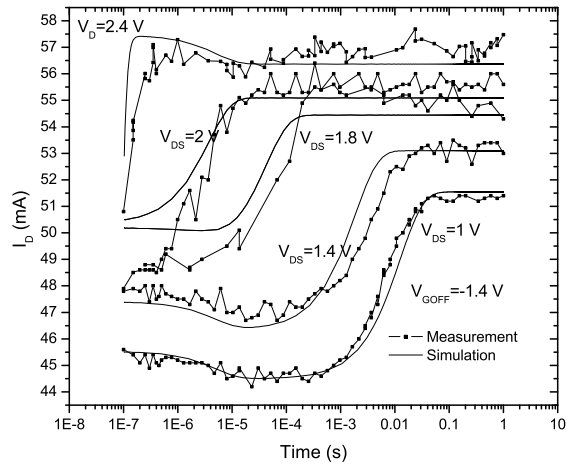


Fig. 7. Comparison of simulated and measured drain current transient for  $V_{G_{OFF}} = -1.4$  V.

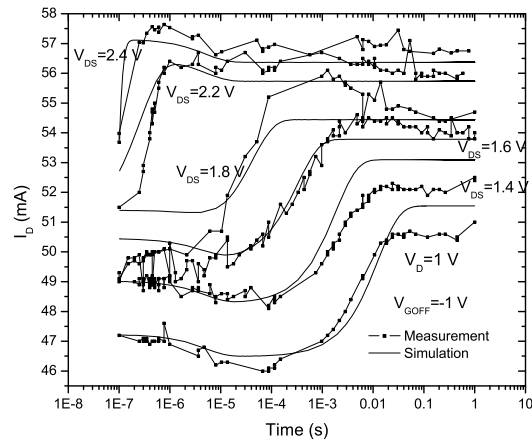


Fig. 8. Comparison of simulated and measured drain current transient for  $V_{G_{OFF}} = -1$  V.

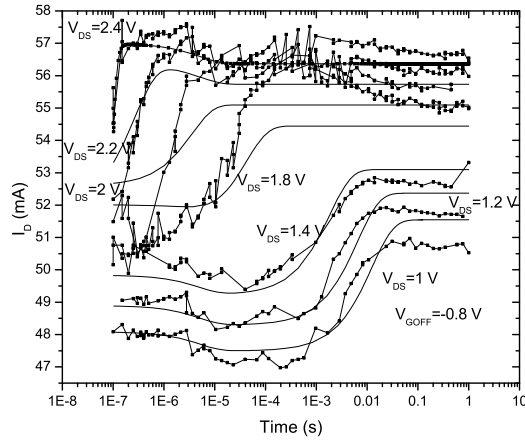


Fig. 9. Comparison of simulated and measured drain current transient for  $V_{G_{OFF}} = -0.8$  V.

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