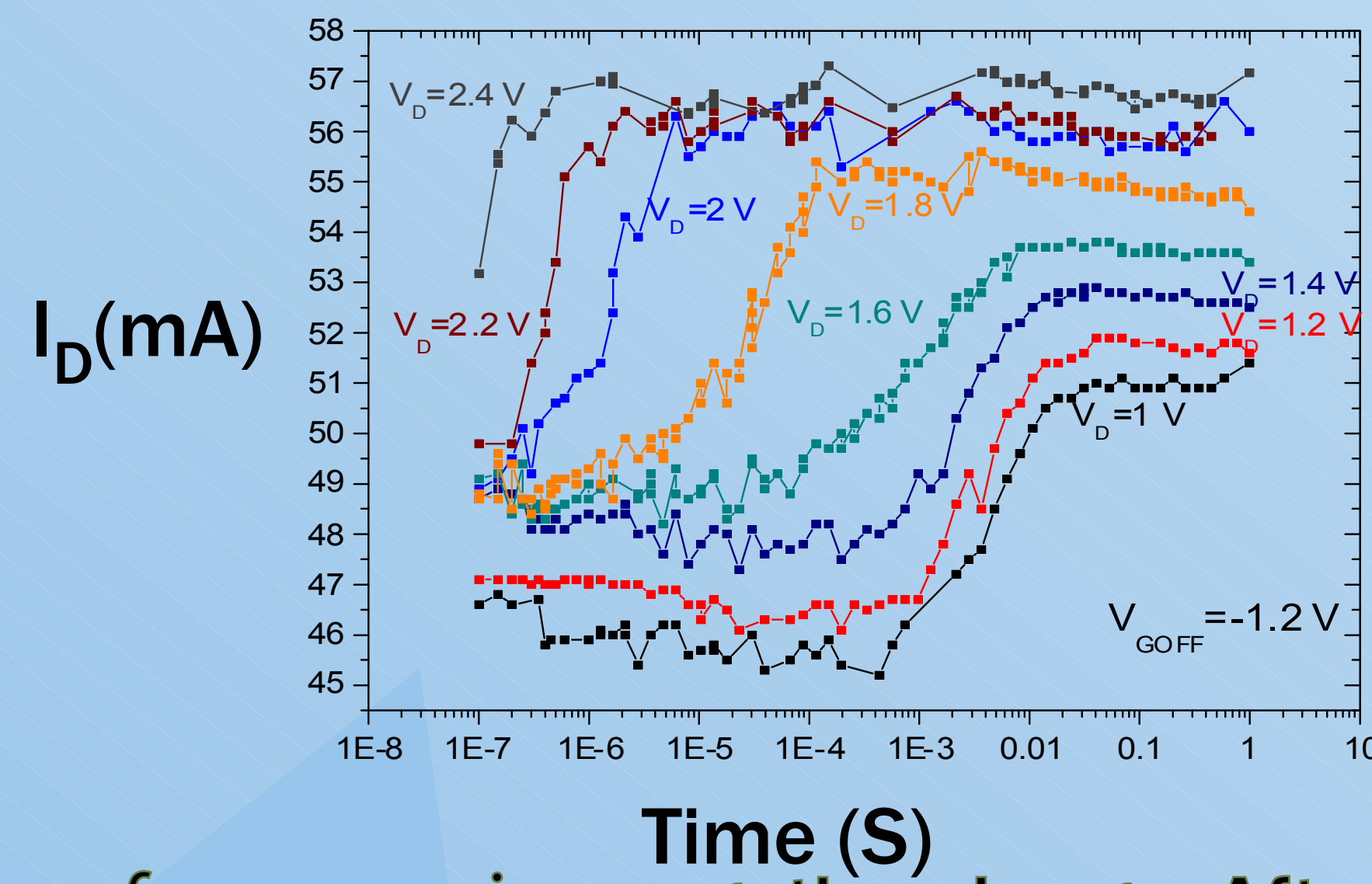
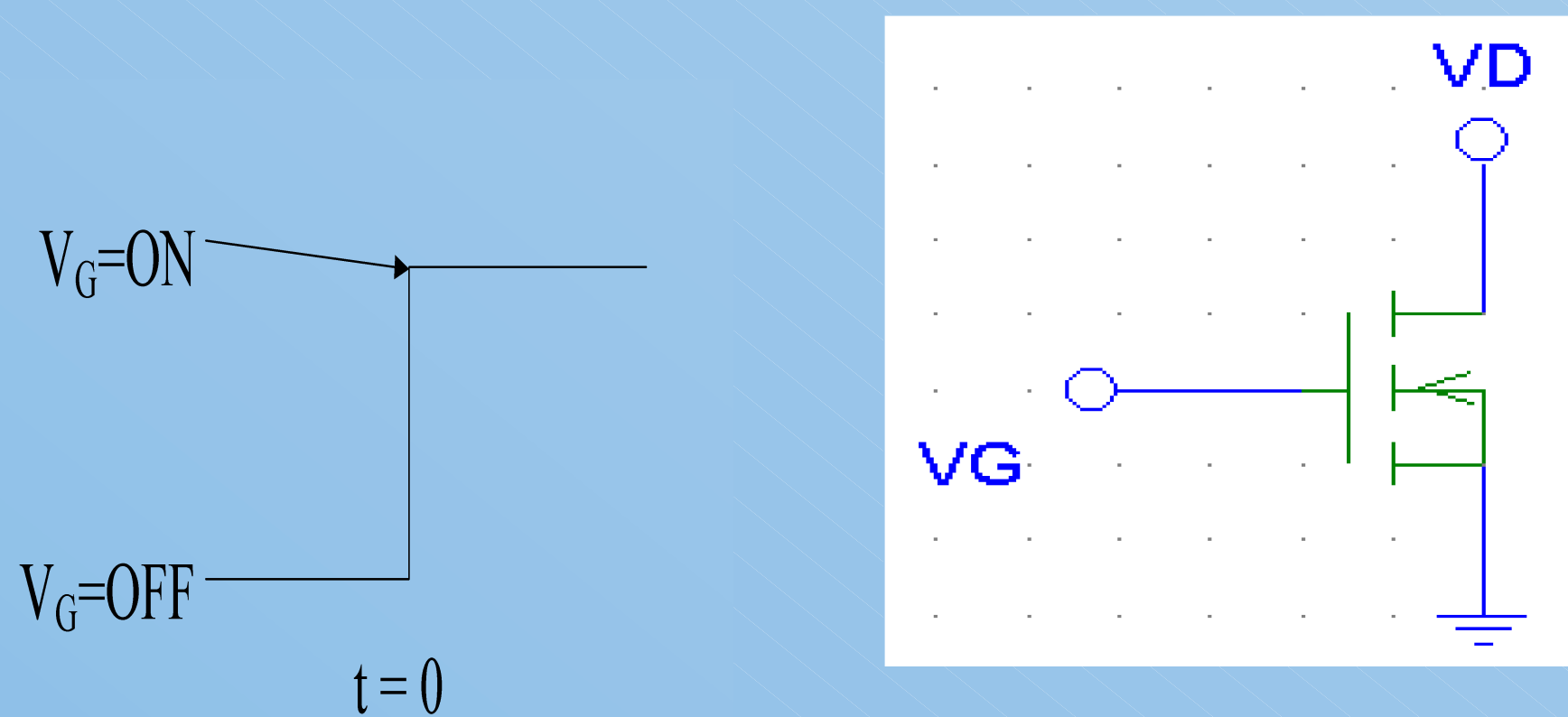


Modeling electron Trapping effects on Gate lag in Field Effect devices

Saif Zaman and Anthony Parker, Department of Electronics, Macquarie University, Sydney

Measurement :

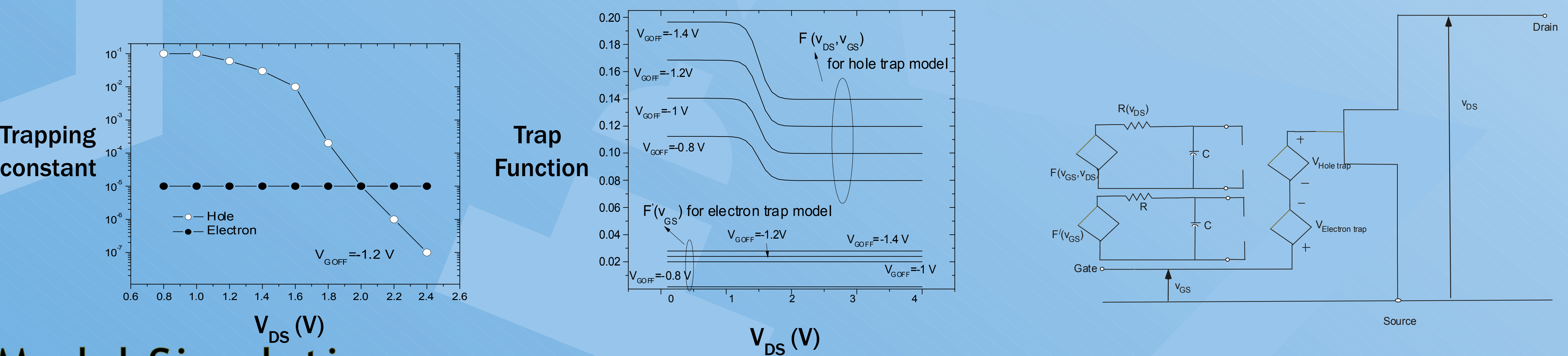
Observation: Delay in transistor Turn On after application of pulse at the gate. Before the rise, there is a slight current fall.



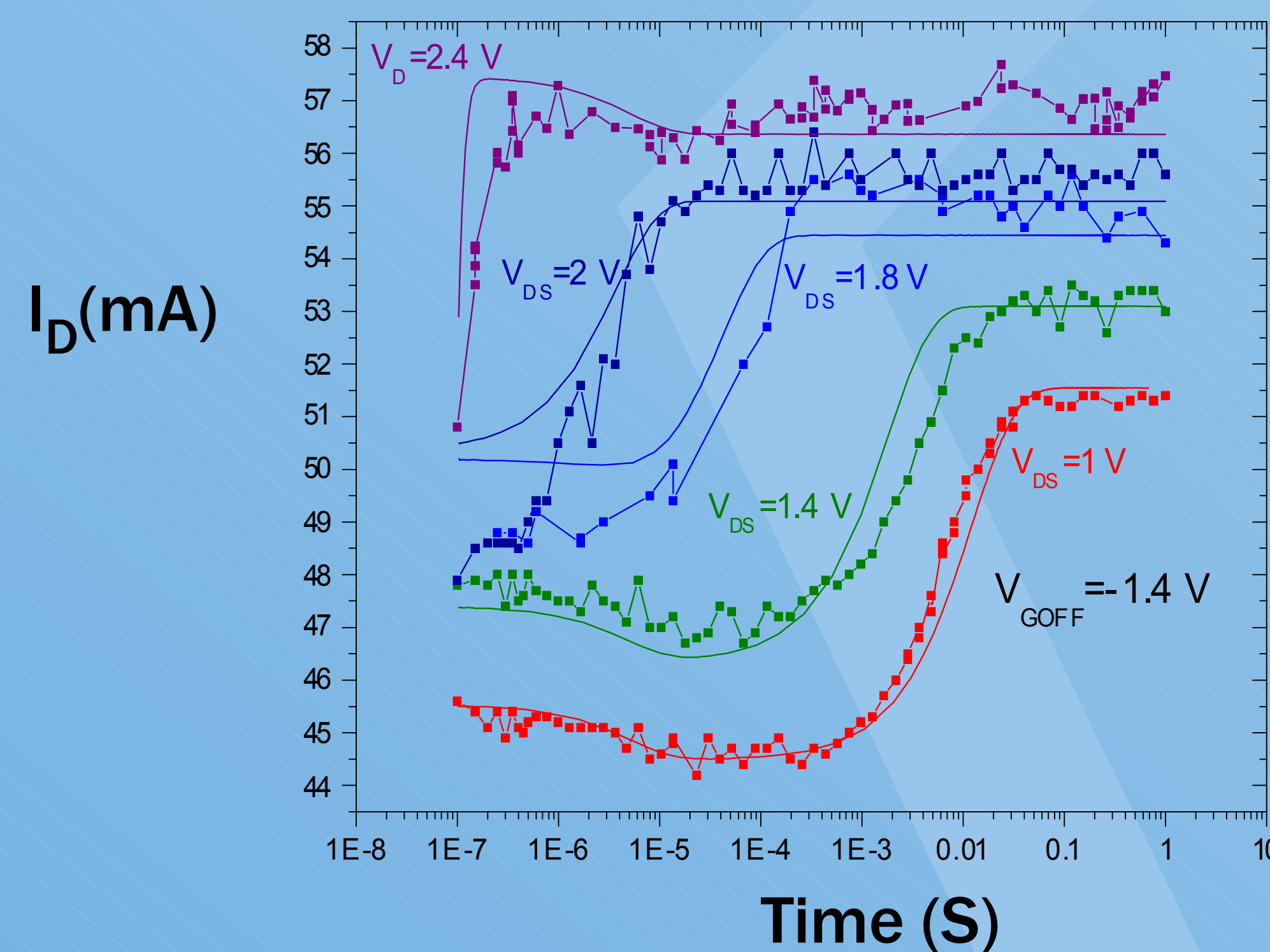
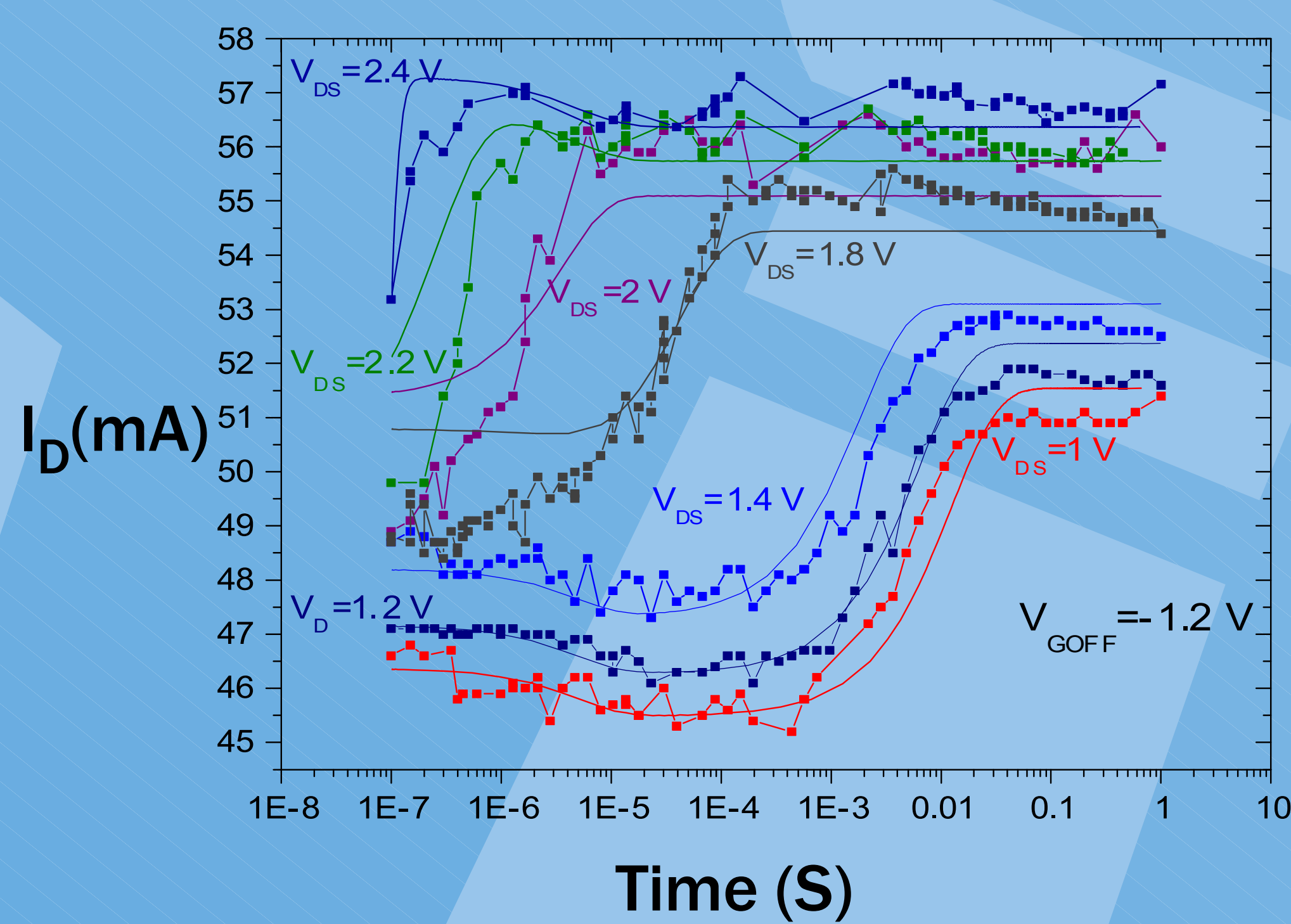
Explanation: When gate is turned off, hole traps at the surface acquire negative charge. After turn-on, this charge decays by capturing holes. The initial fall of current is caused by electron traps that capture channel electron during the turn-on process.

Model:

Description: Hole trap voltage is modeled by a nonlinear gate/drain voltage dependent voltage source, while electron trap voltage has a fixed dependence on gate voltage. The hole trap time constant has a nonlinear drain voltage dependence while electron trap time constant is constant.



Model Simulation:



Future work: Two-tone intermodulation simulation of the model.

